Primary Side Quasi-Resonant Controller with CV/CC Operation and MOSFET Integrated

REV.00

General Description

The LD9162C is an excellent primary side feedback controller with CV/CC operation, integrated several functions of protections. It minimizes the components counts and is available in a tiny SOP-8 package. Those make it an ideal design for low cost applications.

It provides functions of low startup current, green-mode power-saving operation, leading-edge blanking of the current sensing and internal slope compensation. Also, the LD9162C features OTP (Over Temperature Protection) and OVP (Over Voltage Protection) to prevent the circuit being damaged from the abnormal conditions.

In most cases, the power supply with primary-side feedback controller would accompany with some serious load regulation effect. To deal with this problem, the LD9162C consists of dedicated load regulation compensation circuit to improve it.

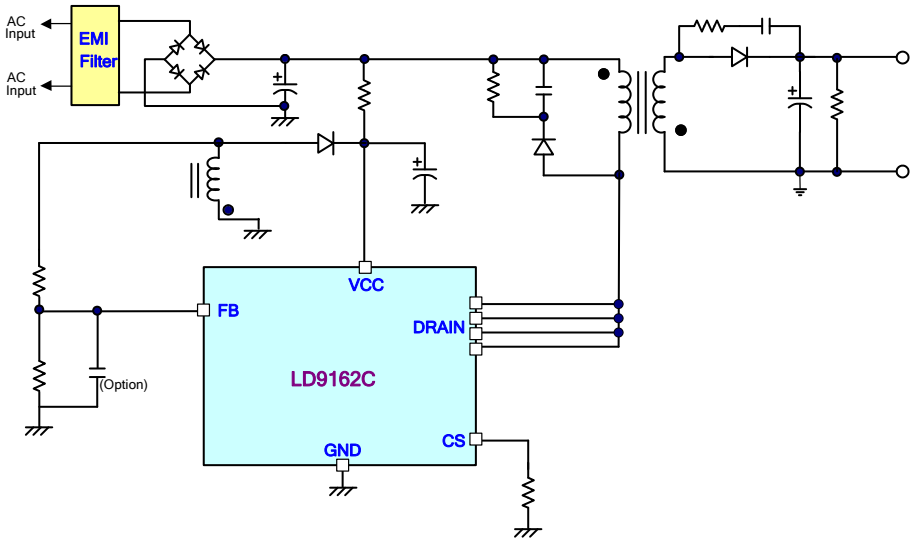
Features

- Primary-side feedback control with quasi-resonant operation
- Built-in 650V/2A MOS Switch
- Built-in Load Regulation Compensation
- Constant current control
- Low Startup Current (<1.5μA)
- 75 kHz Maximum Switching Frequency.
- Current Mode Control with Cycle-by-Cycle Current Limit
- Green Mode Control
- 16V/6.5V UVLO (Under Voltage Lockout)
- LEB (Leading-Edge Blanking) on CS Pin
- VCC OVP (Over Voltage Protection)
- Internal OTP (Over Temperature Protection)

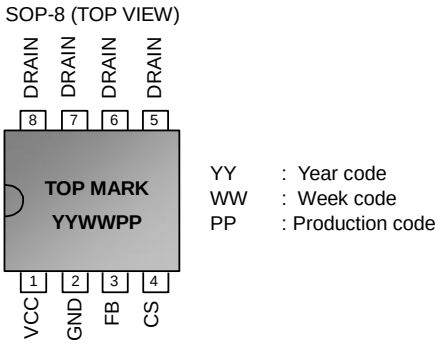
Applications

- USB Charger
- Lower Power AC/DC Adaptor

Typical Application



Pin Configuration



Ordering Information

Part number	Package	TOP MARK	Shipping
LD9162C GS	SOP-8	LD9162C GS	2500 / tape & reel

The LD9162C is ROHS compliant/ Green Packaged.

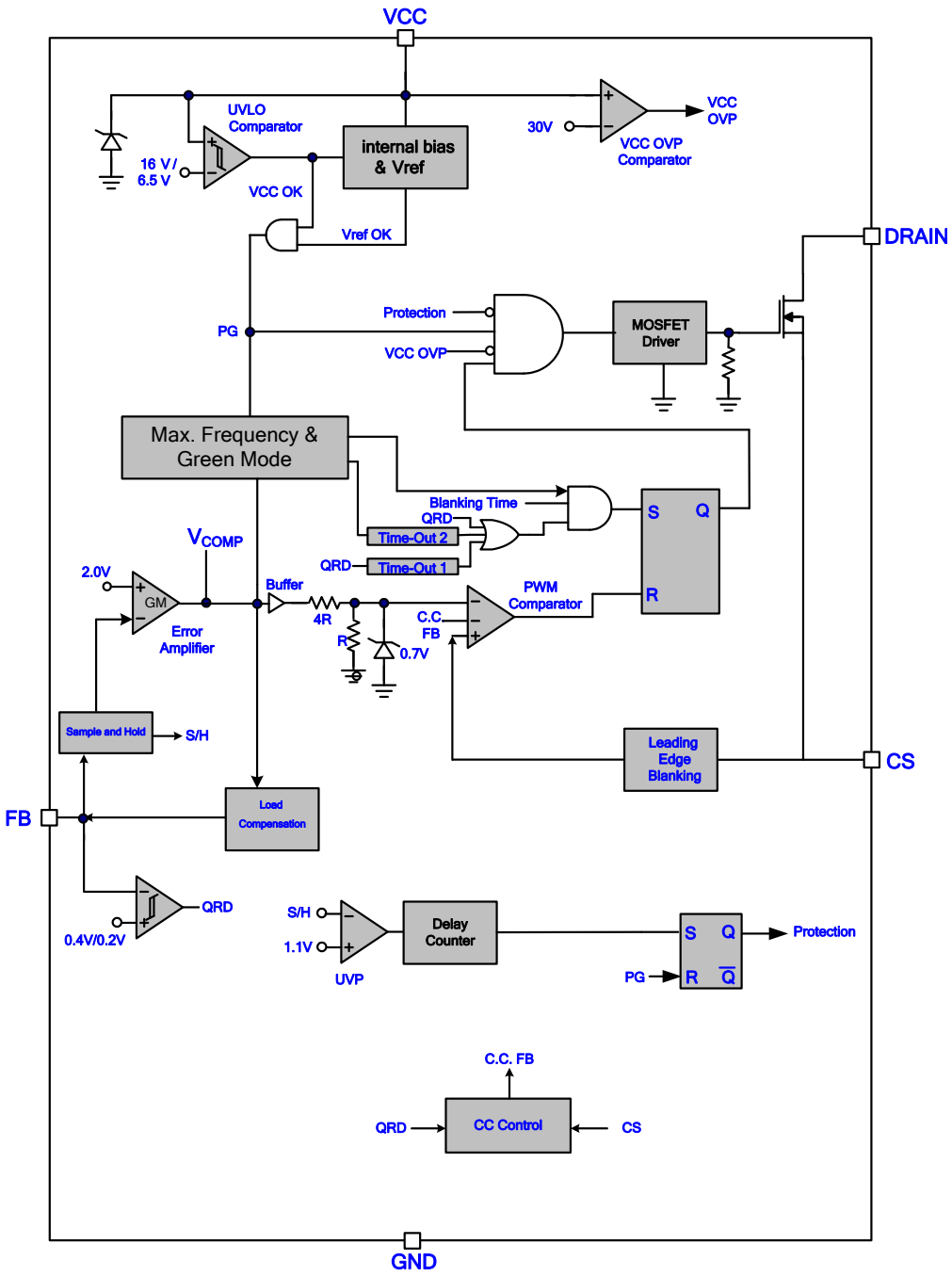
Protection Mode

Part number	VCC_OVP	FB_OVP	FB Open/Short	Internal OTP
LD9162C GS	Auto-Restart	Auto-Restart	Auto-Restart	Auto-Restart

Pin Descriptions

NAME	PIN (SOP-8)	FUNCTION
VCC	1	Supply voltage pin.
GND	2	Ground.
FB	3	Auxiliary voltage sense and Quasi Resonant detection.
CS	4	Current sense pin, connect to sense the switch current.
DRAIN	5/6/7/8	Drain of the integrated MOSFET switch

Block Diagram



Absolute Maximum Ratings

Supply Voltage VCC,	32V
DRAIN	-0.3V ~ 650V
CS	-0.3V ~ 6V
FB (IFB = 6mA @T < 200ns)	-0.8V~3.5V
Maximum Junction Temperature	150°C
Storage Temperature Range	-65°C to 150°C
Package Thermal Resistance (SOP-8, θ_{JA})	106°C/W
Power Dissipation (SOP-8, at Ambient Temperature = 85°C)	377mW
Lead temperature (Soldering, 10sec)	260°C
ESD Voltage Protection, Human Body Model (DRAIN pin is exclusive)	2.5 KV
ESD Voltage Protection, Machine Model (DRAIN pin is exclusive)	250 V

*Note1: The value of θ_{JA} is measured with the device mounted on 1oz one layer FR-4 board, in a still air environment with TA = 25°C. The value in any given application depends on the user's specific board design.

Caution:

Stresses beyond the ratings specified in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Recommended Operating Conditions

Item	Min.	Max.	Unit
Operating Junction Temperature	-40	125	°C
VCC Voltage	9	20	V
Start-up capacitor	2.2	10	μF
AC Start-up resistor	2	6.2	MΩ

Note:

1. It's essential to connect VCC pin with a SMD ceramic capacitor (0.1μF ~ 0.47μF) to filter out the undesired switching noise for stable operation. This capacitor should be placed close to IC pin as possible
2. The small signal components should be placed to IC pin as possible.

Electrical Characteristics

(T_A = +25°C unless otherwise stated, VCC=12.0V)

PARAMETER	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNITS
Supply Voltage (VCC Pin)						
Startup Current	VCC=UVLO-ON-0.05V*	I_{CC_ST}		1	1.9	μA
Operating Current	V_{COMP}=0V, OUT=open*	I_{CC_OP}	0.4	0.7	1	mA
UVLO (OFF)		V_{CC_OFF}	6	6.5	7	V
UVLO (ON)		V_{CC_ON}	15	16	17	V
VCC OVP Level		V_{CC_OVP}	28.5	30	31.5	V
QRD (Quasi Resonant Detection, FB Pin)						
Reference Voltage, V_{REF}		V_{REF}	1.98	2.00	2.02	V
FB OVP Level	*	V_{FB_OVP}		2.5		V
Under Voltage Level	*	V_{FB_UVP}		1.1		V
Current Sense (CS Pin)						
LEB time	*	T_LEB		450		ns
Maximum Input Voltage	*	V_{CS_MAX}	0.67	0.7	0.73	V
Minimum V_{CS}-off	At High Line*	$V_{CS\_MIN\_L}$		0.125		V
Minimum V_{CS}-off	At Low Line*	$V_{CS\_MIN\_H}$	0.15	0.165	0.18	V
Oscillator for Switching Frequency						
Maximum Frequency		F_{S_MAX}	67	75	83	kHz
Minimum Frequency		F_{S_MIN}	0.6	0.7	0.8	kHz
Output Drive (OUT Pin)						
Maximum On Time		T_{ON_MAX}	20	25	32	μs
Internal OTP (Over Temperature)						
OTP Level	*	T_{OTP}		140		°C
OTP Hysteresis	*	T_{OTP_HYS}		22		°C
MOSFET Drain (DRAIN Pin)						
Breakdown Voltage	VGS=0V, ID=250μA	V_{DS}	650			V
On Resistance	VGS=10V, ID=1A	R_{DS_ON}		4.25	5.1	Ω

*: Guaranteed by design

Typical Performance Characteristics

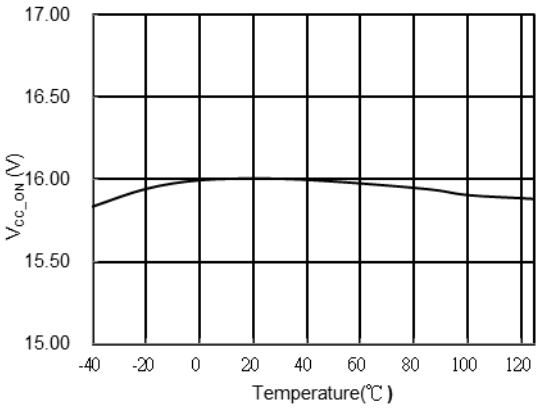


Fig. 1 V_{UVLO_ON} vs. Temperature

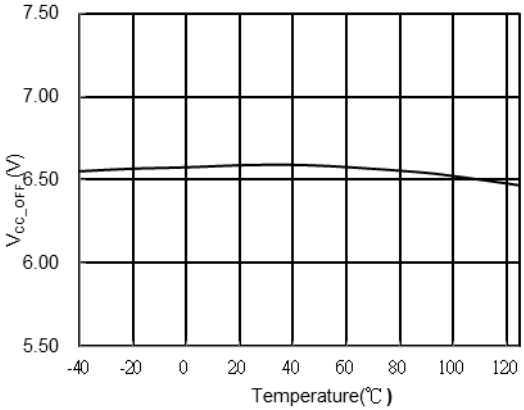


Fig. 2 V_{UVLO_OFF} vs. Temperature

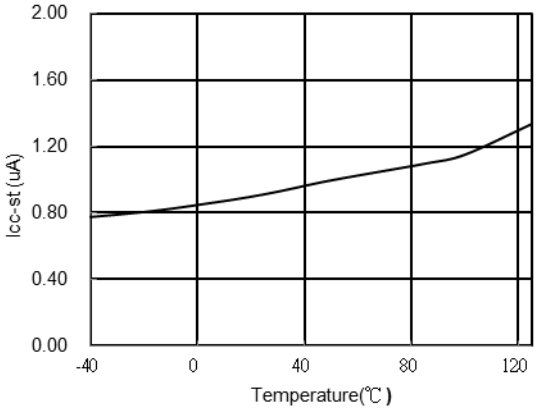


Fig. 3 Startup vs. Temperature

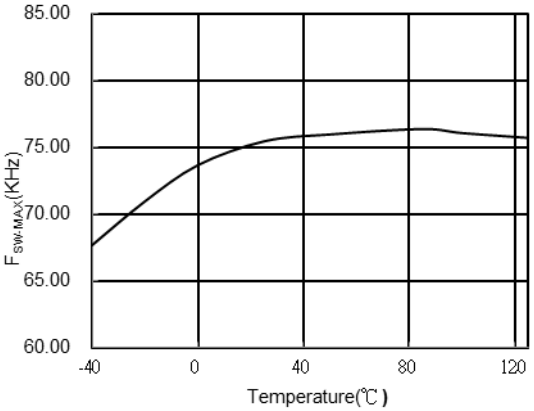


Fig. 4 Max Frequency vs. Temperature

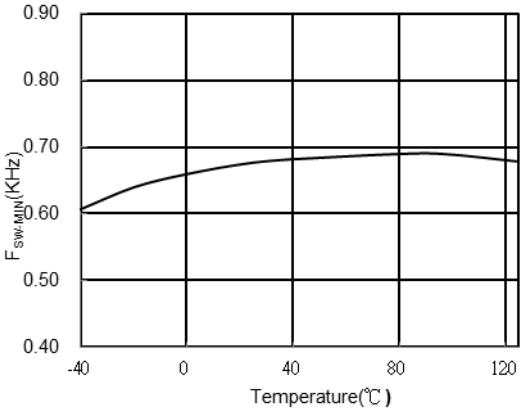


Fig. 5 Min_Frequency vs. Temperature

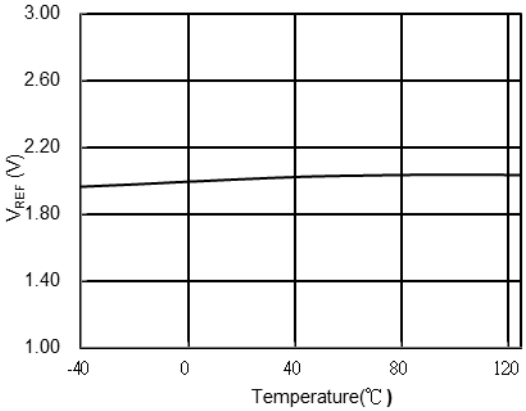


Fig. 6 Reference Voltage vs. Temperature

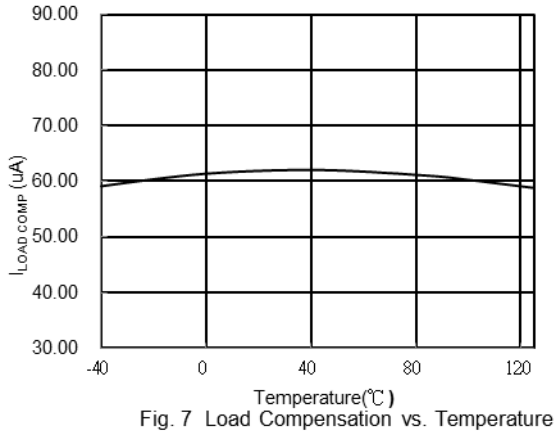


Fig. 7 Load Compensation vs. Temperature

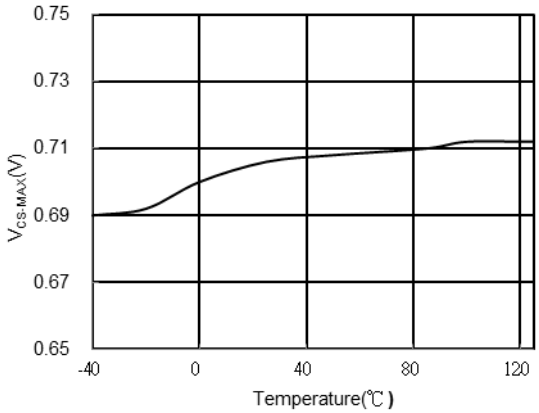


Fig. 8 V_{CS-MAX} vs. Temperature

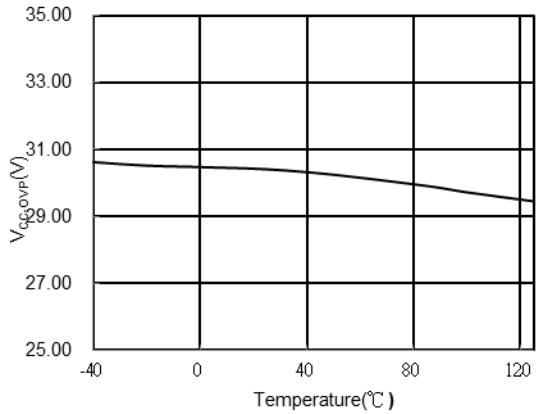


Fig. 9 VCC OVP vs. Temperature

Application Information

Operation Overview

The LD9162C is an excellent primary side feedback controller with quasi-resonant operation to provide high efficiency. The LD9162C removes the need for secondary feedback circuits while achieving excellent line and load regulation. It meets the green-power requirement and is intended for the use in those modern switching power suppliers and linear adaptors that demand higher power efficiency and power-saving. It integrates with more functions to reduce the external components counts and the size. Major features are described as below.

Under Voltage Lockout (UVLO)

An UVLO comparator is implemented in it to detect the voltage across VCC pin. It would assure the supply voltage enough to turn on the LD9162C and further to drive the power MOS. As shown in Fig. 10, a hysteresis is built in to prevent shutdown from voltage dip during startup.

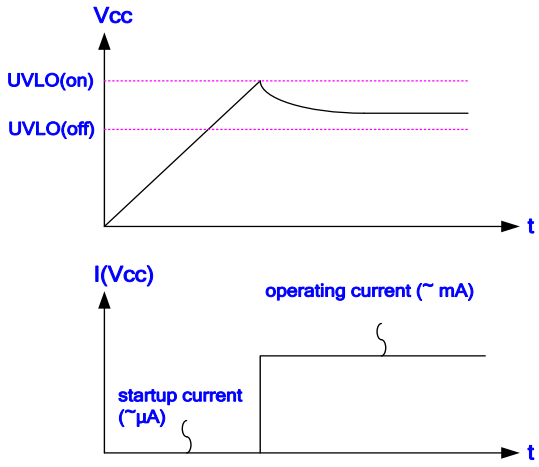


Fig. 10

Startup Current and Startup Circuit

The typical startup circuit to generate VCC of the LD9162C is shown in Fig. 11. At startup transient, the VCC is below the UVLO(ON) threshold, so LD9162C will not work in this condition. Therefore, the current through R1 will be used to charge the capacitor C1. Until the VCC is fully charged to enable the LD9162C to start switching, the auxiliary winding of the transformer will provide supply current. Lower startup current requirement on the PWM controller will help to increase the value of R1 and then reduce the power consumption on R1. By using CMOS process and some unique circuit design, the LD9162C requires only 1.5μA max to start up. Higher resistance of R1 will spend much more time to start up. The user is recommended to select proper value of R1 and C1 to optimize the power consumption and startup time.

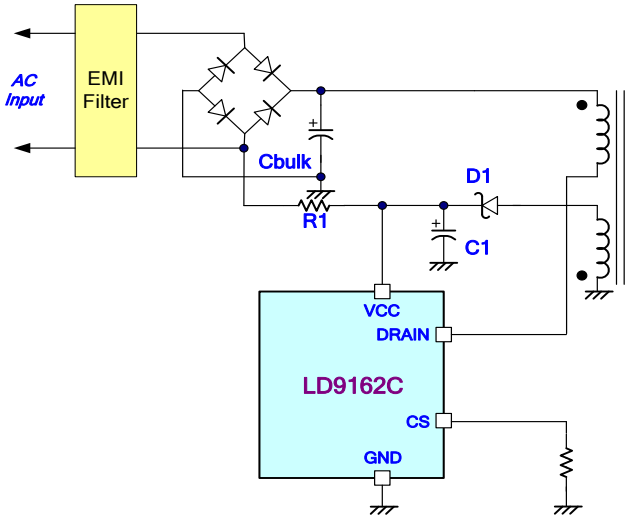


Fig. 11

Principle of CV Operation

In the DCM flyback converter, it can sense the output voltage from auxiliary winding. LD9162C samples the auxiliary winding on the primary-side to regulate the output voltage, as shown in the Fig. 3. The voltage induced in the auxiliary winding is a reflection of the secondary winding

voltage while the MOS is in off state. Via a resistor divider connected between the auxiliary winding and FB pin, the auxiliary voltage is sampled after the sample delay time which is defined as 30~45% of secondary current discharge time from previous cycle. And will be hold until the next sampling period. The sampled voltage is compared with an internal reference V_{REF} (2.0V) and the error will be amplified. The error amplifier output COMP reflects the load condition and controls the duty cycle to regulate the output voltage, thus constant output voltage can be achieved. The output voltage is given as:

$$V_{OUT} = 2.0V(1+\frac{Ra}{Rb})(\frac{Ns}{Na}) - V_F$$

Where V_F indicates the drop voltage of the output diode, Ra and Rb are top and bottom feedback resistor value. Ns and Na are the turns of transformer secondary and auxiliary.

In case that the output voltage is sensed through the auxiliary winding; the leakage inductance will induce ringing to affect output regulation. To optimize the drain voltage clamp circuit will minimize the high frequency ringing and achieve the best regulation. Fig. 13 shows the desired drain voltage waveform in compare to those with large undershoot due to leakage inductance induced ring Fig. 14. The ringing may make the sample error and cause poor performance for output voltage regulation. A proper selection for resistor R_S, in series with the clamp diode, may reduce any large undershoot, as shown in Fig. 12.

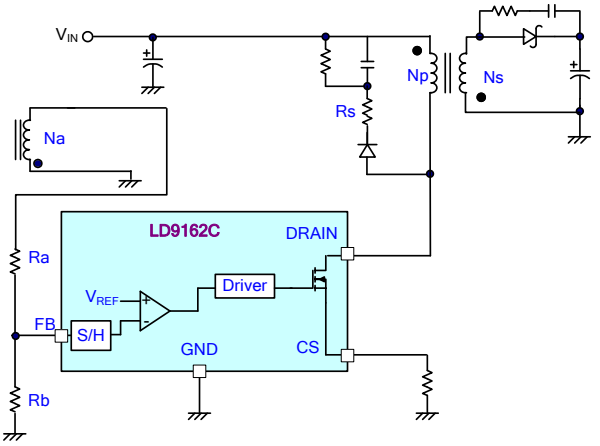


Fig. 12

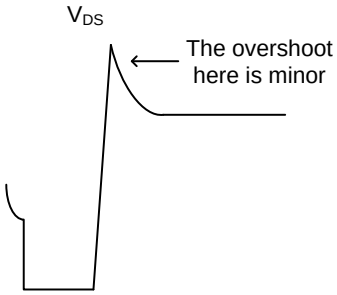


Fig.13

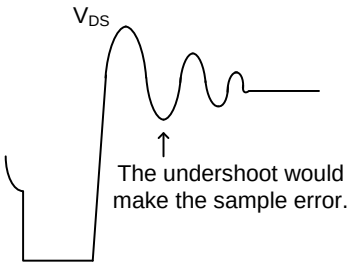


Fig.14

Load Regulation Compensation

LD9162C is implemented with load regulation compensation to compensate the cable voltage drop and to achieve a better voltage regulation. The offset voltage across FB is produced by the internal sink current source during the sampling period. The internal sinking current source is proportional to the value of V_{CS} to compensate

the cable loss as shown in Fig. 15. So, the offset voltage will decrease as the V_{CS} decreases from full-load to no-load. It is programmable by adjusting the resistance of the voltage divider to compensate the drop for cable lines used in various conditions. The equation of internal sink current is shown as:

$$I_{LOAD\_COMP} = (V_{CS} - 0.2) \times 75\,(\mu A)$$

The compensation current versus V_{CS} is shown as:

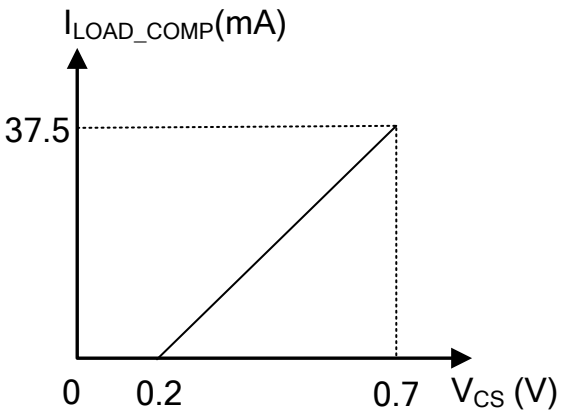


Fig. 15

Quasi-Resonant Mode Detection

The LD9162C employs quasi-resonant (QR) switching scheme to switch in valley-mode either in CV or CC operation. This will greatly reduce the switching loss and the ratio dv/dt in the entire operating range for the power supply. Fig. 16 shows the typical QR detection block. The QR detection block will detect auxiliary winding signal to drive MOS as FB pin voltage drops to 0.2V. The QR comparator will not activate if FB pin voltage remains above 0.4V.

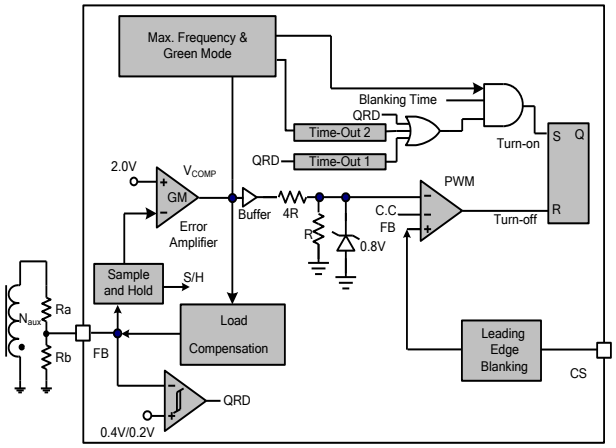


Fig. 16

Multi-Mode Operation

The LD9162C is a QR controller operating in multi-modes. The controller changes operation modes according to line voltage and load conditions. At heavy-load, there might be two situations to meet. If the system AC input is in low line, the LD9162C will turn on in first valley. If in high line, the switching frequency will increase till over the limit of 75 kHz and skip the first valley to turn on in 2nd, 3rd….valley. The switching frequency would vary depending on the line voltage and the load conditions when the system is operated in QR mode.

At medium load conditions (operation frequency about 25 kHz ~ 45 kHz), the frequency is clamped between green mode frequency and maximum frequency. However, the characteristic in valley switching behaves well without problem in this condition. The LD9162C will turn on in 4th, 5th…. valley. That is, when the load decreases, the system will automatically skip some valleys and the switching frequency is therefore reduced.

Current Sensing and Leading-Edge Blanking

The typical current mode of PWM controller feedbacks both current signal and voltage signal to close the control

loop and achieve regulation. As shown in Fig. 3, the LD9162C detects the primary MOS current from the CS pin, which is not only for the peak current mode control but also for the pulse-by-pulse current limit. The maximum voltage threshold of the current sensing pin is set at 0.7V. From above, the MOS peak current can be obtained from below.

$$I_{PEAK(MAX)} = \frac{0.7V}{R_S}$$

A leading-edge blanking (LEB) time about 450ns is included in the input of CS pin to prevent the false-trigger from the turn-on current spike.

High/Low Line Detection

LD9162C has setting the high/low line detect voltage through (Ra). Assume that V_{HL_H} is the boundary voltage between high/low line detect level. The equation of Ra is shown as:

$$R_a = \frac{V_{HL\_H} \times \sqrt{2} \times \frac{N_a}{N_P}}{600\mu A}$$

The high line current as 600μA, according to the Ra value the C.C. compensation will adjust at different lines voltage.

Principle of C.C. Operation

The primary side control scheme is applied to eliminate secondary feedback circuit or opto-coupler, which will reduce the system cost. The switching waveforms are shown in Fig. 17. The output current "Io" can be expressed as:

$$Io = \frac{1}{2}\frac{i_{S,PK} \times T_{DIS}}{T_S}$$
$$= \frac{1}{2}\frac{N_P}{N_S} \times i_{P,PK} \times \frac{T_{DIS}}{T_S}$$
$$= \frac{1}{2}\frac{N_P}{N_S} \times \frac{V_{CS}}{R_{CS}} \times \frac{T_{DIS}}{T_S}$$

The primary peak current ($i_{P,PK}$), inductor current discharge time (T_{DIS}) and switching period (T_S) can be detected by the IC. The ratio of $V_{CS*}T_{DIS}/T_S$ will be modulated as a constant ($V_{CS*}T_{DIS}/T_S$ =1/3). So that I_O can be obtained as

$$Io = \frac{1}{2}\frac{N_P}{N_S} \times \frac{V_{CS}}{R_S} \times \frac{T_{DIS}}{T_S}$$
$$= \frac{1}{2}\frac{N_P}{N_S} \times \frac{1}{R_S} \times \frac{1}{3}$$

However this is an approximate equation. The user may fine-tune it according to the experiment result.

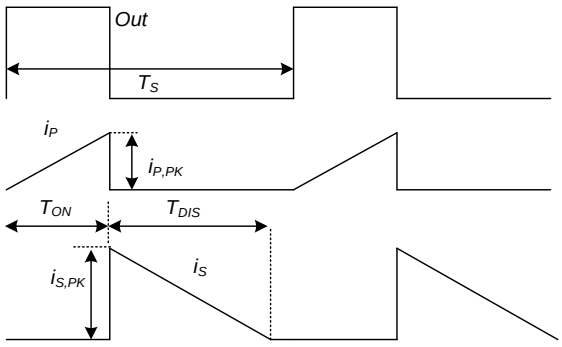


Fig. 17

OVP (Over Voltage Protection) on VCC – Auto Recovery

LD9162C is implemented with OVP function through VCC. As the VCC voltage rises over the OVP threshold voltage, the output drive circuit will be shut off simultaneously thus to stop the switching of the power MOS until the next UVLO (ON) arrives. The VCC OVP function of LD9162C is an auto-recovery type protection. The Fig. 18 shows its operation. That is, if the OVP condition is removed, it will resume to normal output voltage and VCC level in normal condition.

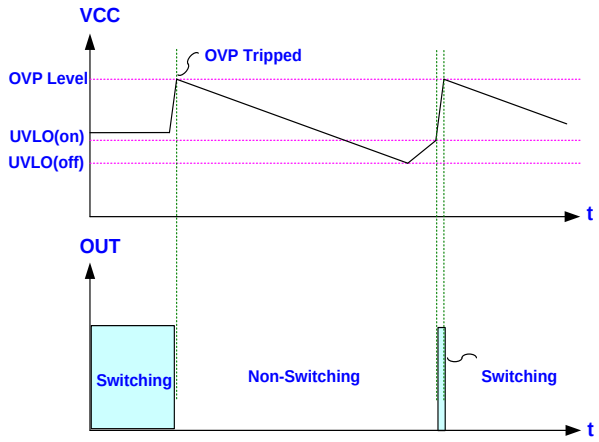


Fig. 18

FB Under Voltage Protection (FB UVP) & FB Short Circuit Protection – Auto Recovery

LD9162C is implemented with an UVP function over FB pin. If the FB voltage falls below UVP level over the delay time (20ms), the protection will be activated to stop the switching of the power MOS until the next UVLO (ON) arrives. The FB UVP function in LD9162C is an auto-recovery type protection. The Fig. 19 shows its operation. During the soft start period, the FB UVP is disabled to avoid output under UVP level in soft start period. In soft start period, the Fig. 20 shows the operation. While FB is short to GND, FB pin keeps in zero voltage level. If FB cannot detect any voltage signal over 0.2V in the beginning of soft start period, then the soft start will turn to generate a driving signal every 1.5ms until FB UVP delay to shut down IC and auto recovery.

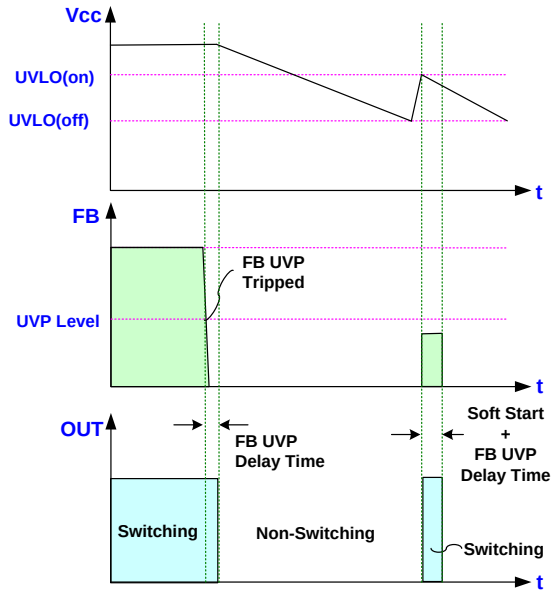


Fig. 19

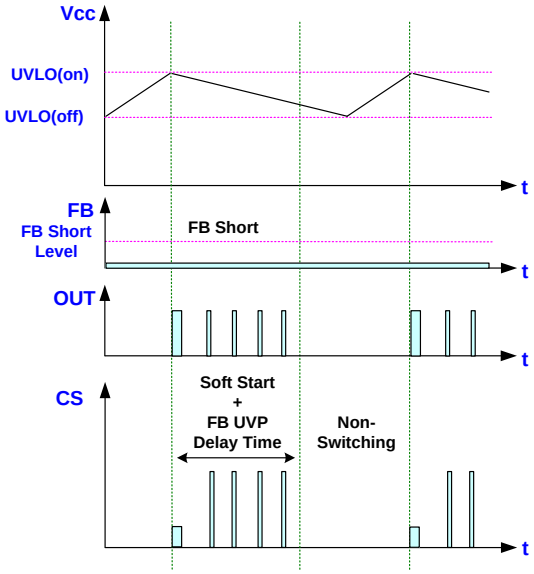
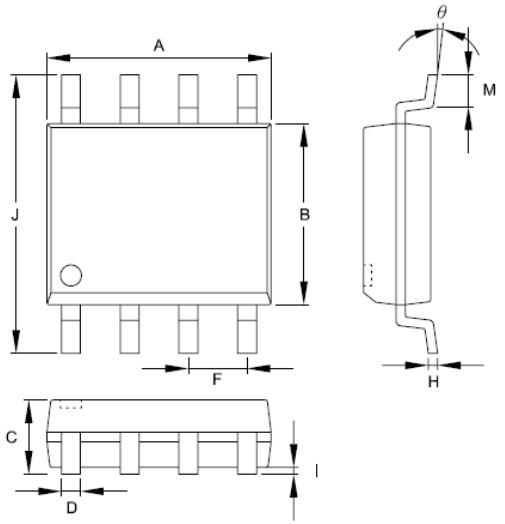


Fig. 20

Package Information

SOP-8



Symbols	Dimensions in Millimeters		Dimensions in Inch	
	MIN	MAX	MIN	MAX
A	4.801	5.004	0.189	0.197
B	3.810	3.988	0.150	0.157
C	1.346	1.753	0.053	0.069
D	0.330	0.508	0.013	0.020
F	1.194	1.346	0.047	0.053
H	0.178	0.254	0.007	0.010
I	0.102	0.254	0.004	0.010
J	5.791	6.198	0.228	0.244
M	0.406	1.270	0.016	0.050
θ	0°	8°	0°	8°

Important Notice

Leadtrend Technology Corp. reserves the right to make changes or corrections to its products at any time without notice. Customers should verify the datasheets are current and complete before placing order.

Revision History

Rev.	Date	Change Notice
00	03/02/2018	Original Specification